2019 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon 2019
ATTENDEE QUESTIONNAIRE RESULTS

ATTENDEES' PRIMARY JOB FUNCTIONS

System Design	21%
Standard IC Design	9%
ASIC /SoC Design	37%
DSP Design	6%
Microprocessor/Microcontroller Design	8%
IP Development	19%
Analog/Mixed Signal	12%
EDA Methods & Tools	32%
Verification	61%
FPGAs & PLDs	15%
Software/Embedded Software	15%
Safety Design	4%
Machine Learning / AI hardware design	15%
Student	1%

ATTENDEES' JOB DESCRIPTIONS

Senior Management	15%
Engineering Management	11%
Design Engineer	11%
System Architecture	3%
Application Engineer	7%
Marketing	3%
Technical Marketing	3%
Product Marketing	2%
Sales	5%
Research/Academic	3%
CAD	3%
Verification Engineer	29%
Software Engineer	3%
Student	1%

SIZE IN GATES OF ATTENDEES' CURRENT/LAST DESIGN

Not Applicable	47%
<1M	7%
1M - 5M	6%
5M - 10M	4%
10M - 50M	7%
50M - 100M	5%
100M - 500M	7%
500M - 1B	6%
1B - 2B	4%
> 2B	7%

VERIFICATION LANGUAGE USED BY EITHER ATTENDEE OR FUNCTIONAL VERIFICATION TEAM

Verilog	48%
VHDL	16%
C/C++	36%
SystemC	18%
SystemVerilog	66%
e	4%
Not Applicable	20%

VERIFICATION METHODOLOGY USED BY FUNCTIONAL VERIFICATION TEAM

UVM	55%
OVM	1%
VMM	1%
eRM	0%
SystemC/TLM	4%
Portable Stimulus (PSS)	3%
Proprietary	9%
I am not involved	27%

FIRST-TIME ATTENDEE

Yes	35%
No	65%