2020 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon 2020
ATTENDEE QUESTIONNAIRE RESULTS

ATTENDEES' PRIMARY JOB FUNCTIONS

System Design	21%
Standard IC Design	7%
ASIC /SoC Design	31%
DSP Design	4%
Microprocessor/Microcontroller Design	10%
IP Development	19%
Analog/Mixed Signal	9%
EDA Methods & Tools	29%
Verification	59%
FPGAs & PLDs	16%
Software/Embedded Software	15%
Safety Design	5%
Machine Learning / AI hardware design	15%
Student	1%

ATTENDEES' JOB DESCRIPTIONS

Senior Management	16%
Engineering Management	14%
Design Engineer	7%
System Architecture	3%
Application Engineer	5%
Marketing	3%
Technical Marketing	3%
Product Marketing	2%
Sales	5%
Research/Academic	1%
CAD	2%
Verification Engineer	33%
Software Engineer	4%
Safety Engineer	0%
Student	1%

SIZE IN GATES OF ATTENDEES' CURRENT/LAST DESIGN

Not Applicable	47%
<1M	6%
1M - 5M	6%
5M - 10M	4%
10M - 50M	6%
50M - 100M	4%
100M - 500M	6%
500M - 1B	4%
1B - 2B	5%
> 2B	11%

VERIFICATION LANGUAGE USED BY EITHER ATTENDEE OR FUNCTIONAL VERIFICATION TEAM

Verilog	48%
VHDL	16%
C/C++	41%
SystemC	20%
SystemVerilog	70%
e	5%
Not Applicable	17%

VERIFICATION METHODOLOGY USED BY FUNCTIONAL VERIFICATION TEAM

UVM	46%
OVM	6%
VMM	2%
eRM	1%
SystemC/TLM	10%
Portable Stimulus (PSS)	7%
Proprietary	9%
I am not involved	18%

FIRST-TIME ATTENDEE

Yes	35%
No	65%