DVCon 2014 Demographic Totals

1. Which verification language is used by your functional verification team? (Pick one)	
Verilog	17%
VHDL	2%
C/C++	8%
SystemC	4%
SystemVerilog	50%
Not Applicable	20%

2. Which primary verifcation language do you currently use? (Pick one)	
C/C++	11%
e	2%
OpenVera	0%
Verilog	11%
VHDL	2%
SystemC	3%
System Verilog	50%
Not Applicable	20%

3. Which primary verification language do you plan to use for your next design? (Pick one)	
C/C++	9%
e	2%
OpenVera	0%
Verilog	8%
VHDL	1%
SystemC	5%
SystemVerilog	54%
Not Applicable	21%

4. Which verification methodology is used by your functional verification team?	
UVM	51%
OVM	5%
VMM	3%
eRM	1%
SystemC/TLM	3%
Home Grown	9%
Other	5%
I am not involved	23%

5. Which primary property specification (assertion-based verification) language do you use or plan to use?	
Verilog	26%
VHDL	4%
PSL	4%
SystemVerilog (SVA)	67%

6. What area(s) are you focused on? (Check all that apply)	
Systems Design	27%
Standard ICs	10%
ASICs	41%
DSP Design	8%
Microprocessor/Microcontroller Design	17%
FPGAs & PLDs	23%
Multi-Chip Modules	4%
PCBs	4%
Library Development	4%
Analog/Mixed Signal	11%
EDA Tools	35%
Verification	52%
SOCs	34%
Software/Embedded Software	15%

7. What on-chip buses do you intend to use in the next 12 months?	
AMBA 2.0 AHB/APB	28%
AMBA 3 AXI	33%
OCP 2.0	4%
OCP 2.1	4%
CoreConnect	4%
Others/Proprietary	26%
None	35%

8. What interfaces standards do you expect to use in the next 12 months?	
PCI Express 1.1	8%
PCI Express 2.0	33%
USB 2.0/OTG	13%
USB 3.0	25%
Serial ATA	10%
10G Ethernet	15%
10/100/1G Ethernet	20%
Wireless USB	6%
PCI/PCI-X	8%
CE-ATA	1%
None	45%

DVCon 2014 Demographic Totals
(continued)

9. What is the size in gates of your current/last design? (Pick one)	
Not Applicable	38%
<1M	8%
1 - 3M	6%
3 - 5M	4%
5 - 10M	10%
10M - 50M	15%
>50M	19%

10. How many clock domains do your designs average?	
1	4%
2	5%
2 -5	20%
5 - 10	12%
10 - 20	12%
>20	11%
Not Applicable	36%

11. What is your number one design constraint?	
Low power	42%
Size/density	12%
Performance/throughput	46%

12. What are the two main reasons for your attendance at DVCon?	
Learn new techniques to improve your design process	34%
Learn new methodologies to improve your verification process	53%
Learn about new developments in design tools	37%
Meet and network with other engineers in the industry	46%
Learn about industry in general	35%

13. Which category most closely describes your job description? (Pick one)	
Senior Management	15%
Unsubscribe	36%
Engineering Management	17%
Design Engineer	10%
System Architecture	4%
Application Engineer	4%
Marketing	3%
Technical Marketing	3%
Product Marketing	3%
Sales	3%
Research/Academic	3%
CAD	3%
Verification Engineer	28%
Software Engineer	3%